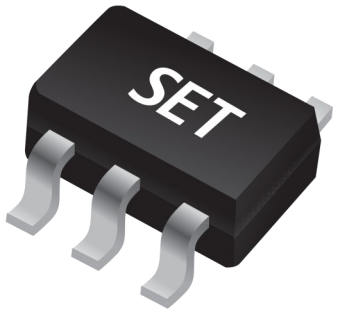
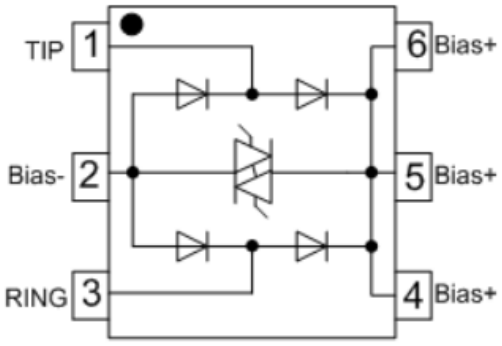


Schematic & Pinout Configuration



Description

SIP5024G is a type of semiconductor silicon protection device with integrated circuit design inside to achieve a capacitive loading characteristic that is compatible with these high bandwidth applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals from damaging overvoltage transients.

SIP5024G is in a compact surface mount SOT23-6 package which provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of tertiary protectors.

Features

- Compact and low profile package
- Low capacitance and leakage current
- Low clamping voltage
- Compatible with VDSL2、ADSL2
- Balanced overvoltage protection
- Response time under 500 ns
- Low insertion loss
- Low distortion
- Moisture sensitivity level: Level 3
- Flammability Rating: UL 94 V-0
- Halogen free and RoHS compliant

Order Information

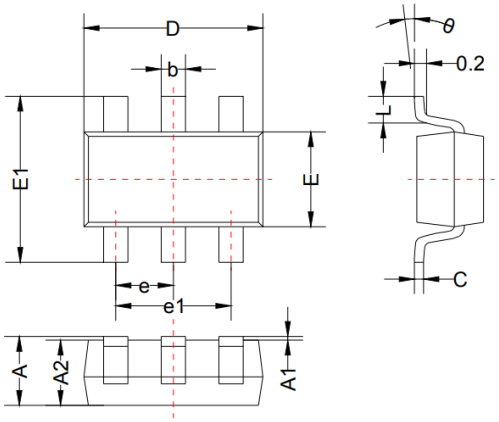
Type	Package	Marking Code	Delivery Form	Delivery Quantity
SIP5024G	SOT23-6	J24G	7” T&R	3000 PCS

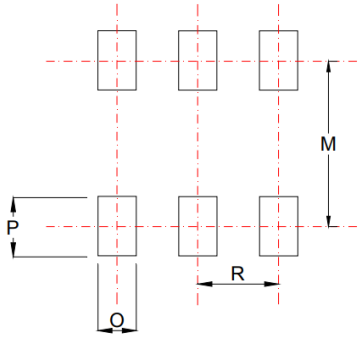
Limiting Values

(T_A = 25 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	Electrostatic Discharge Voltage	IEC 61000-4-2; Contact Discharge	-	8	kV
		IEC 61000-4-2; Air Discharge	-	15	kV
I_{PP}	Non-repetitive impulse current	t_P=8 / 20 μs	-	35	A
T_L	Lead soldering temperature	260 (10 sec.)		260	°C
T_A	Operating Temperature Range	-	-40	150	°C
T_{stg}	Storage Temperature Range	-	-65	150	°C

Package Dimensions

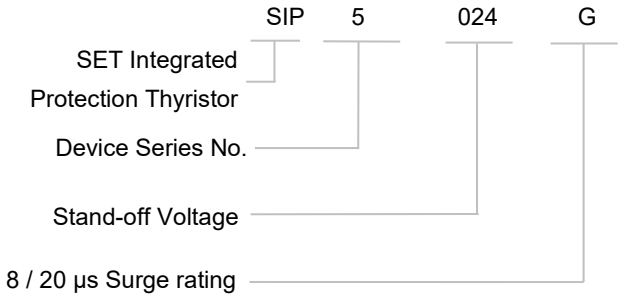




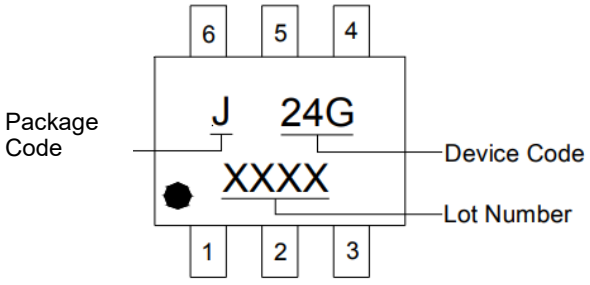
Recommended solder pad layout

Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.05	1.25	0.041	0.049
A1	0.00	0.10	0.000	0.004
A2	1.05	1.15	0.041	0.045
B	0.30	0.50	0.012	0.020
C	0.10	0.20	0.004	0.008
D	2.85	3.05	0.112	0.120
E	1.50	1.70	0.059	0.067
E1	2.65	2.95	0.104	0.116
e	0.95 BSC		0.037 BSC	
e1	1.80	2.00	0.071	0.079
L	0.30	0.60	0.012	0.024
θ	0 °	8 °	0 °	8 °
M	-	2.59	-	0.102
O	-	0.69	-	0.027
P	-	0.99	-	0.039
R	-	0.95	-	0.038

Part Numbering System (Example)



Marking



Electrical Characteristics

(T_A = 25 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{DRM}	Stand-off Voltage	I_{DRM} = 1 μA	24	-	-	V
I_{DRM}	Off-state Leakage Current	V_{DRM} = 24 V	-	-	1	μA
V_s	Switching Voltage	100 kV / s	-	30	-	V
I_S	Switching Current	-	10	-	-	mA
I_H	Holding Current	-	-	40	-	mA
V_T	On-state Voltage	I_T = 1 A I_T = 1 A, pin 5 to pin 2	-	-	3.5 1	V
V_C	Clamping Voltage	I_{PP} = 35 A, t_P=8 / 20 μs	-	32	35	V
C_o	Off-state Capacitance	Bias Voltage =2 V, f = 1 MHz	-	1.1	3.0	pF
ΔC_O	Delta Off-state Capacitance	Line Bias =1 V to V_{DRM}	-	-	0.5	pF

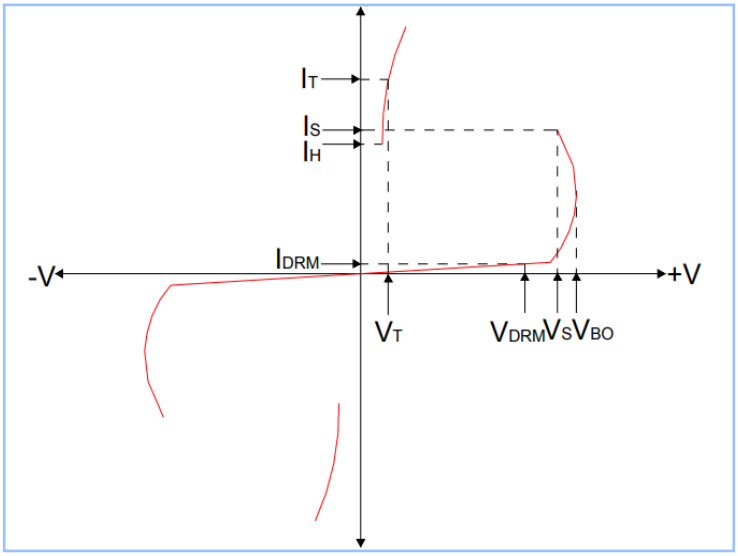
Note :

All measurements made between pin 1 and pin 3 unless otherwise stated.

Electrical Characteristics

(T_A = 25 °C, unless otherwise specified)

Symbol	Parameter
V_{DRM}	Peak off-state voltage
I_{DRM}	Off-state current
V_S	Switching voltage
I_S	Switching current
V_T	On-state voltage
I_T	On-state current
I_H	Holding current
C_O	Off-state capacitance



Performance Curve for Reference

(T_A=25 °C unless otherwise noted)

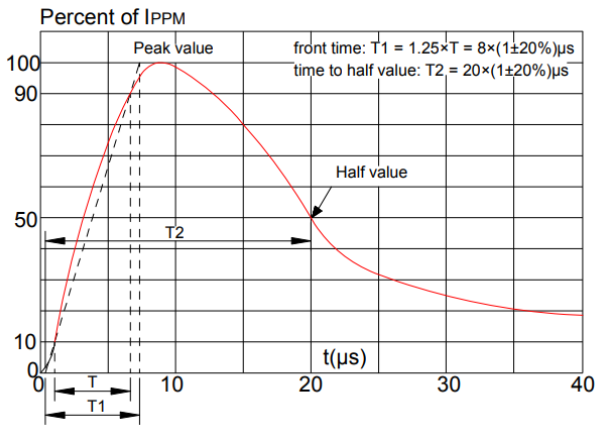


FIGURE 1

tr × td Pulse Waveform (8 / 20 μs)

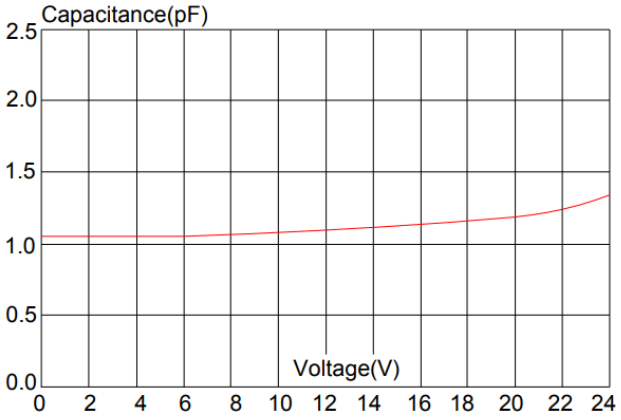


FIGURE 2

Typical capacitance against line voltage (without external bias)

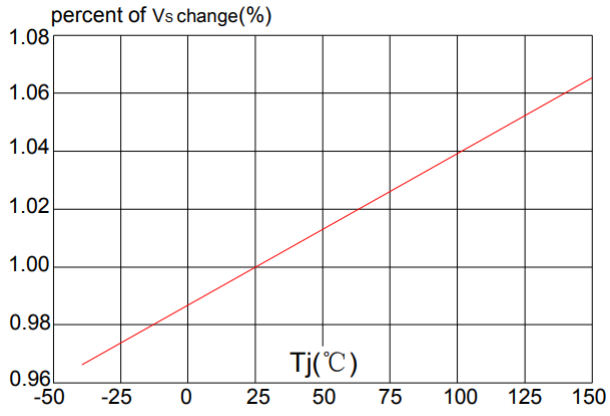


FIGURE 3

Normalized VS. Change VS. Junction Temperature

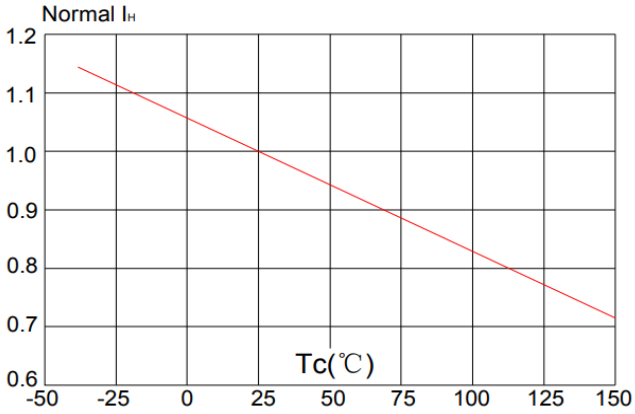
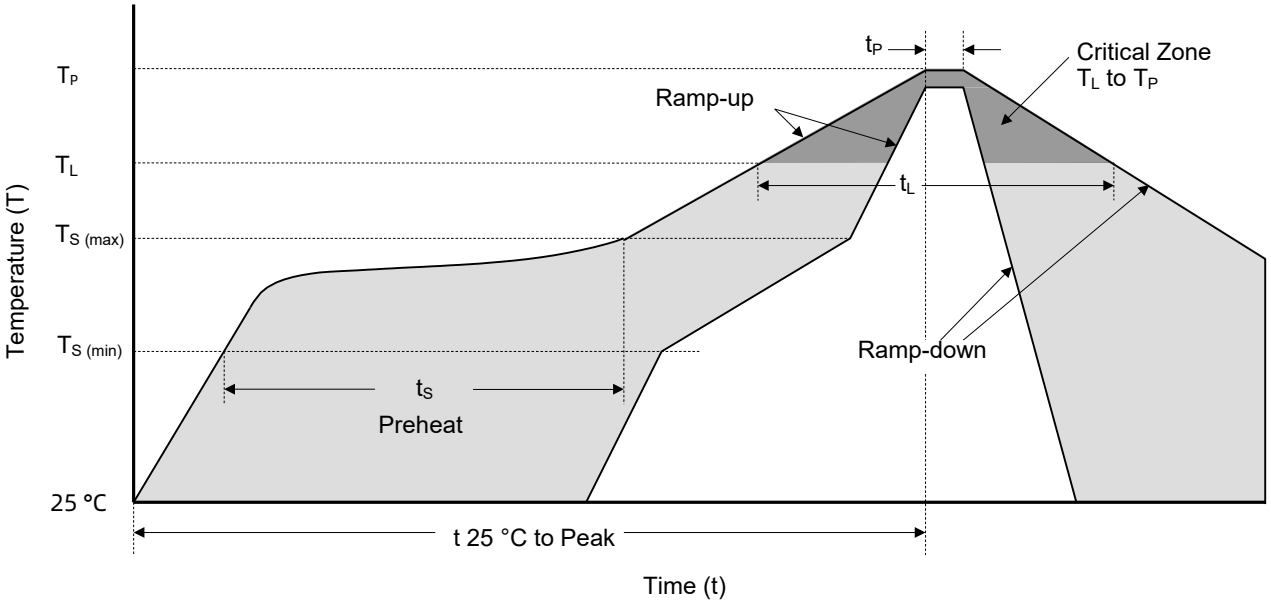


FIGURE 4

Normalized Holding Current VS. Case Temperature

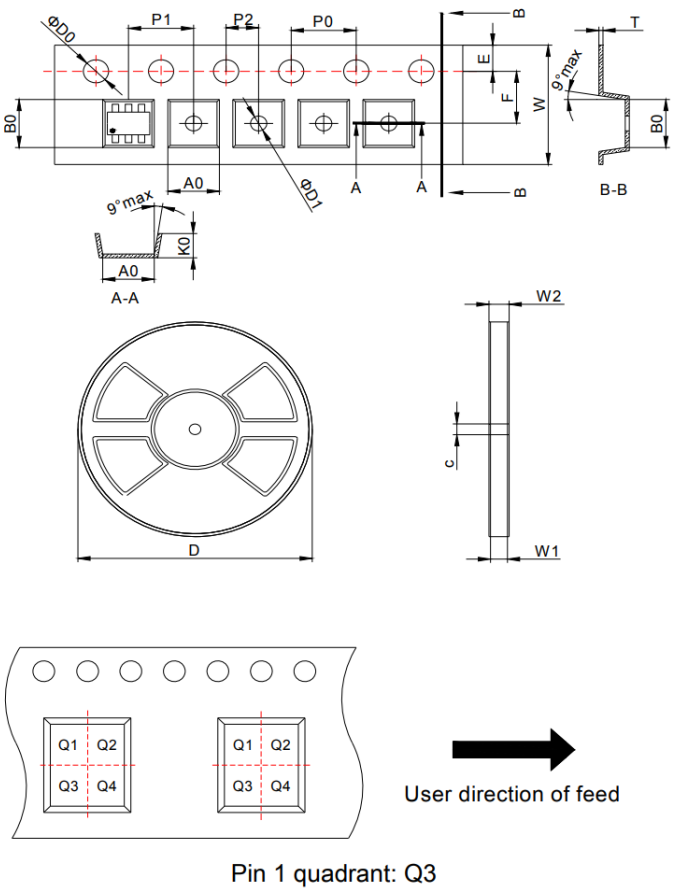
Soldering Parameters



Reflowing Condition

Reflow Soldering Parameters		Lead-Free Assembly
Pre-heat	Temperature Min ($T_{S\ (min)}$)	150 °C
	Temperature Max ($T_{S\ (max)}$)	200 °C
	Time (min to max) (t_s)	60 ~ 120 seconds
Average Ramp Up Rate (Liquidus Temp (T_L) to Peak Temp (T_P))		3 °C / second max.
T_S (max) to T_L-Ramp-up Rate		3 °C / second max.
Reflow	Temperature (T_L)	217 °C
	Time (t_L)	60 ~ 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time of within 5 °C of Actual Peak Temperature (t_P)		30 seconds
Ramp-down Rate		6 °C / second max.
Time From 25 °C to Peak Temperature		8 Minutes max.
Do Not Exceed		260 °C

Packaging Information



Pin 1 quadrant: Q3

Symbol	Millimeters	Inches
W	8.0 + 0.30 / - 0.10	0.315 + 0.012 / - 0.004
P1	4.0 ± 0.10	0.157 ± 0.004
E	1.75 ± 0.10	0.069 ± 0.004
F	3.5 ± 0.05	0.138 ± 0.002
D0	Φ1.55 ± 0.05	Φ0.061 ± 0.002
D1	Φ1.0 + 0.25 / - 0.00	Φ0.039 + 0.010 / - 0.000
P0	4.0 ± 0.10	0.157 ± 0.004
P2	2.0 ± 0.05	0.079 ± 0.002
A0	3.17 ± 0.10	0.125 ± 0.004
B0	3.23± 0.10	0.127 ± 0.004
K0	1.37 ± 0.10	0.054 ± 0.004
T	0.25 ± 0.02	0.010 ± 0.001
D	177.80	7.000
W1	10.40 ± 2.00	0.409 ± 0.079
W2	16.20 ± 1.80	0.638 ± 0.071
c	13.25 ± 0.25	0.522 ± 0.010

Part Number	Package	QTY (Reel)	Packaging Option	Packaging Specification
SIP5024G	SOT23-6	3000 PCS	Tape & Reel – 8 mm tape/7” reel	EIA STD RS-481

ATTENTION

Usage

1. TSS must be operated in the specified ambient temp..
2. Do not clean the TSS with strong polar solvent such as ketone, esters, benzene and halogenated hydrocarbon, to avoid damaging the encapsulating layer.
3. Please do not apply severe vibration, shock or pressure to TSS, to avoid element cracking.

Replacement

1. If TSS is visually damaged, please replace it.
2. TSS is a non-repairable product. For safety sake, please use equivalent TSS for replacement.

Storage

1. Storage Temp. Range: (-55 to 150) °C.
2. Do not store the TSS at the high temp., high humidity or corrosive gas environment, to avoid influencing the solder- ability of the lead wires. The product shall be used up within 1 year after receiving the goods.

Environmental Conditions

1. TSS should not be exposed to the open air, nor direct sunshine.
2. TSS should avoid rain, water vapor or other condition of high temp. and high humidity.
3. TSS should avoid sand dust, salt mist, or other harmful gases.

Max. Typical Capacitance of TSS

The typical capacitance of TSS is listed in the specifications. Designers may refer to it when designing TSS in High frequency circuit.

Installation Mechanical Stress

1. Do not knock TSS when installing, to avoid mechanical damage.
2. Please do not apply severe vibration, shock or pressure to TSS, to avoid surface resin or element cracking.